17.3 A 40-to-800MHz Locking Multi-Phase DLL

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The increasing demand for processing large amounts of information has driven developments in high-capacity storage media such as HD-DVD and Blu-ray discs, and continues to drive the industry to seek new optical-storage formats [1,2]. With the evolution of optical storage, circuit technologies have been sought to enable high-speed read/write channel operation. To support down-compatibility from Blu-ray to CD/DVD with various writing speeds, PLLs in the write strategy channel should provide wide lock ranges and should generate multiple phases for precise control of the write pulse-widths.

High-gain VCOs are generally used to achieve wide lock ranges in PLLs [3]. To improve jitter performance with low-gain VCOs, the switching of multiple VCOs [4] and folding of the loop-filter output [2] have been proposed. The multiple VCO scheme, however, requires efficient control for the takeover between VCOs, and the folding scheme needs to use additional analog techniques for smooth transitions around folding points. One limiting factor regarding the multiphase generation at high frequencies is the tightened timing margin. With N evenly-spaced phases, and assuming a clock period of T, the pulse-width is programmed with a time step of T/N with a step error of less than $\pm T/2N$. For example, to support 12× Blu-ray with 20 phases, the step error should be less than 31ps since the maximum frequency is 792 MHz. In addition, generating multiple phases also limits high-frequency operation. For generating N phases, the number of delay stages should be at least N or $N/2$ when used with inverter-type cells or differential cells, respectively. So the maximum lock frequency is limited by the considerable delay of the fixed stages. This paper proposes a DLL-based approach with two enabling circuit schemes, a delay matrix with integrating resistor network and a gradual switching of shunt capacitors.

Figure 17.3.1 shows the block diagram of the DLL. Unlike conventional DLLs, the voltage-controlled delay line is implemented with a delay matrix which enables high-frequency locking as well as the generation of multiple phases. The five outputs of the interpolators differ in time delay by 1/5 of the replica delay and serve as inputs of the 5×8 delay matrix. The delay matrix generates 41 outputs, ϕ_0 through ϕ_{40}. Since ϕ_{40} is delayed by one clock-period from ϕ_0, ϕ_0 and ϕ_{40} are used as inputs to the phase detector. The control bias generation block converts the charge pump output into control voltages for wide-range operation.

Figure 17.3.2 shows the delay matrix with the front-end interpolator stage. An offset delay, Δ, represents the minimum delay required for the interpolation. Assuming the unit delay is τ, the interpolators generate five seed inputs with relative delays of 0τ, 0.2τ, 0.4τ, 0.6τ and 0.8τ, which are applied to five independent 8-stage delay chains. The delay chains are linked through a resistor network so that every pair of neighboring phases is connected by a resistor. Therefore the 5×8 delay matrix generates 40 evenly spaced phases. Since there are only 8 delay cells in each chain, the minimum delay is greatly reduced.

The resistor network performs phase error averaging by providing an additional current path only when a phase error occurs. A similar averaging technique with resistor strings was originally proposed to reduce the effect of comparator offsets in flash ADCs [5]. This work proposes a new phase-error averaging technique with a resistor network so that phase error could be further reduced as the signal propagates through the stages. The first dummy stage is added for the averaging of phase error due to the imperfections of the front-end interpolation, and the last dummy stage for matching the output loading. In this work, the unit resistor is 1KΩ.

Figure 17.3.3 shows how the resistor network achieves averaging if mismatch between delay cells induces phase error. At the time around the signal transition, the delay cells are supposed to generate evenly spaced voltage levels when no error exists. If mismatch induces error, the outputs of the delay cells are different from the expected node voltages of the resistor string. Thus, additional current flows and averages out the phase error. But, when no error exists, the effects of the resistor string are negligible.

Figure 17.3.4 shows the bias circuits for the wide-range control of delay. Each delay cell is a cascade of two identical current-starved inverters with 6 control inputs, *VCn*, *VCp*, *Vn1*, *Vp1*, *Vn2* and *Vp2*. The 6 control voltages are translated from *Vctrl*, the output of the charge pump. To achieve wide-range delay variation, the inverter simultaneously uses two methods of controlling the delay. One method is to control the driving current by *VCn* and *VCp*, and the other is to control the variable shunt capacitance by *Vn1*, *Vp1*, *Vn2*, and *Vp2*. The bias for the pull-down current, *VCn*, is analog-buffered *Vctrl* except for a *Vtp*-clamped transformation. The *Vtp*-clamping prevents the delay cell from completely turning off when *Vctrl* is low enough in low-frequency locking. To achieve a continuous change in the delay, the switches connected to the MOS capacitors are turned on gradually as *Vctrl* decreases so that the inverters see a continuously increasing capacitive loading. To generate the switch control voltages, a low-gain amplification scheme is needed from the *Vctrl* input. To achieve the minimum delay for high-frequency operation, the switches must be completely turned off when *Vctrl* is high enough. Conventional low-gain amplifier schemes, however, can not be used for this purpose since they do not have a full 0-to-V_{DD} output swing. In this work, a gain-suppressed full-swing inverter is used. The transition region is widened by separate low-gain control of the pull-up and pull-down devices. To increase the range of gradual variation of the capacitive loading, two-step switching is also used as shown in the transfer curve. The threshold voltages of the low-gain inverters are separately adjusted by sizing.

The DLL was implemented in a 0.13μm CMOS technology (Fig. 17.3.7). The active area was 550μm×400μm including the 40-to-1 multiplexer for the individual phase measurements. Simple inverters were used for buffers. The DLL generates 40 phases with step errors of less than $\pm T/80$ for the frequency range of 40 to 700MHz at a supply voltage of 1.2V. Figure 17.3.5 shows measured waveforms for the 40 phases. For clarity, two separate windows were taken to show 20 phases in each. Figure 17.3.6 shows the phase linearity characteristics. The dashed lines denote the maximum tolerable error boundaries of $\pm T/80$. The worst delay step error was measured to be 16.7ps at 700MHz. When only every other 20 phases are considered instead of all 40, the DLL has a lock range of up to 800MHz with a maximum delay step error of 25ps, which is less than $\pm T/40$. Since 20 phases can also be used in a typical write-strategy channel, the DLL satisfies 12× Blu-ray speed. The DLL consumes 43mW at 700MHz. The measured peak-to-peak jitter and rms jitter were 12ps and 1.6ps, respectively.

References:

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[2] Y. Konno et al., "A CMOS 1×-16× Speed DVD Write Channel IC," *IEEE J.Solid-State Circuits*, pp.642-650, Mar., 2006.
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[5] K. Kattmann and J. Barrow, "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," *ISSCC Dig. Tech. Papers*, pp.170-171, 1991.

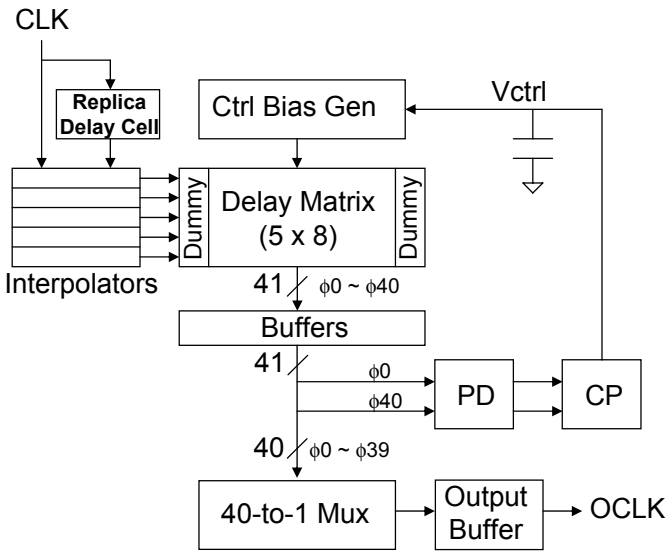

Figure 17.3.1: Block Diagram of the DLL.

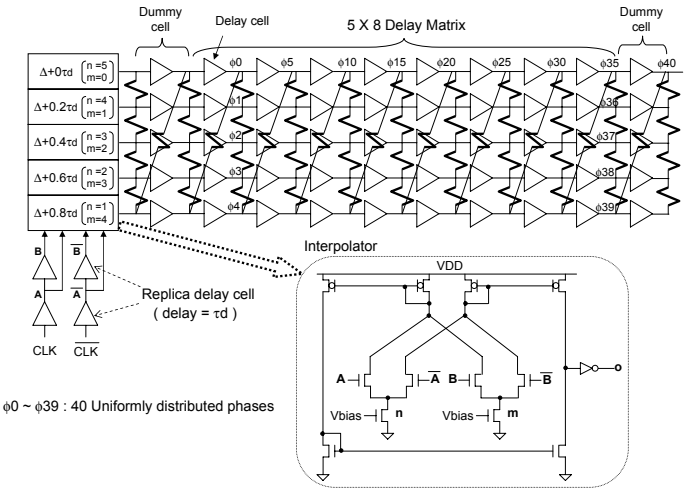

Figure 17.3.2: 5×8 Delay Matrix with Interpolators Generating 40 Phases.

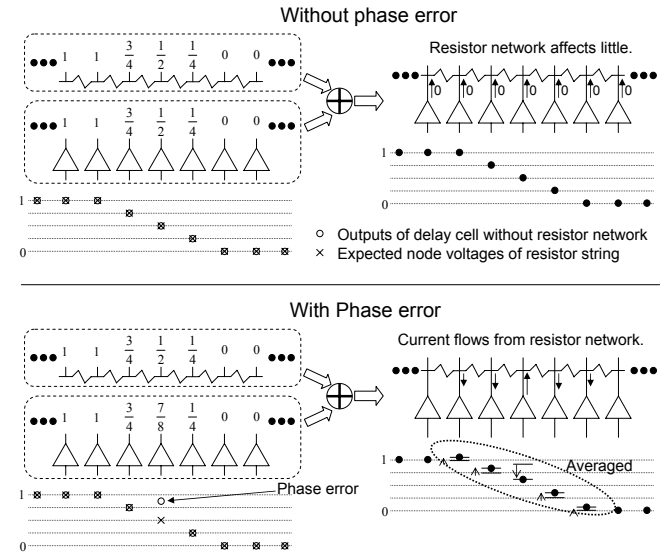

Figure 17.3.3: Conceptual Illustration of Phase Error Averaging.

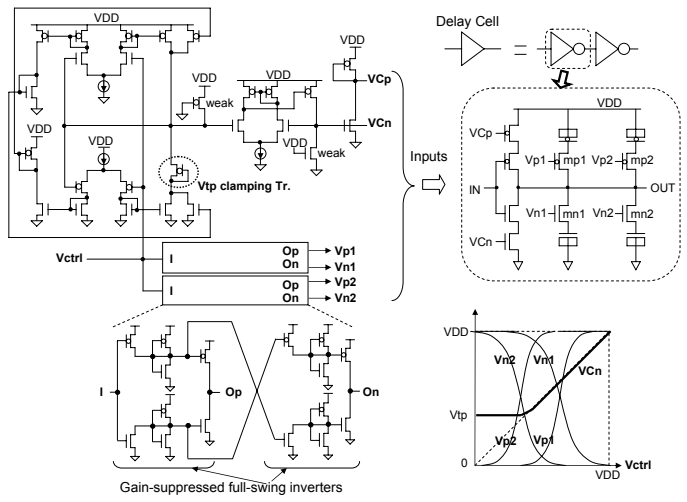

Figure 17.3.4: Bias Circuits for the Delay Cells.

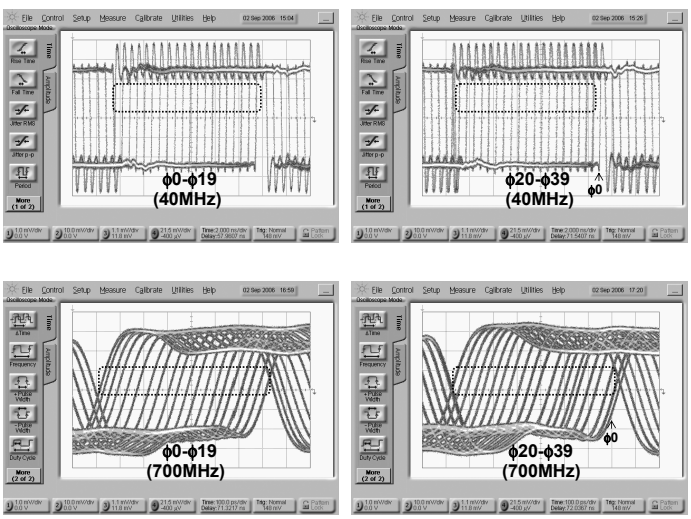

Figure 17.3.5: Measured waveforms for the 40 phases.

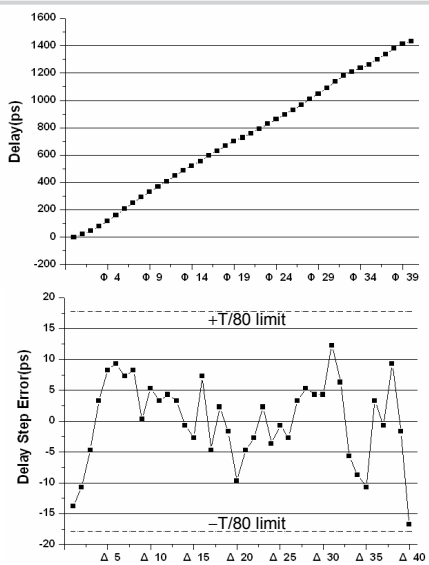

Figure 17.3.6: Phase Linearity Characteristics at 700MHz.

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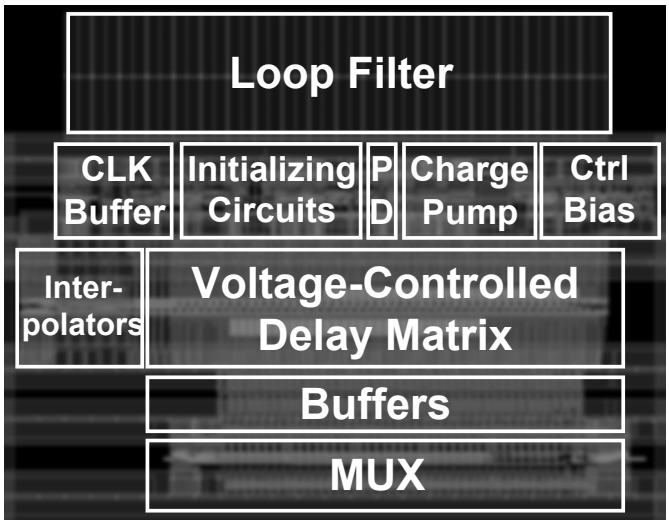

Figure 17.3.7: Micrograph of the fabricated DLL.

